A Force-Directed placement algorithm with simultaneous Global Routing for Sea-of-Gates

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Abstract

An automatic layout tool for placement of macrocells using sea-of-gates architecture is presented. The system uses a hierarchical approach in which the macrocells are placed in slices with the global routing being performed simultaneously with the placement. The system implements a constructive Force-Directed (FD) algorithm based on a physical analogy with an electrostatic model in which the sets of macrocells generate pseudo capacitors in the array image. This approach also takes into consideration the connectivity, routability and geometric aspects of the macrocells in the early stages of the physical design, the aim being to produce more refined layouts with no need for post-processing. This technique aims:

- to avoid post-processing to solve overlapping problems, which is traditional in FD-methodology and increases computation;
- to improve the chip area simultaneously with the placement;
- to allocate enough tracks in early stages of the placement to enhance the routability dynamically during the construction of slices.

1. Introduction

Sea-of-gates[1, 2, 5, 7] technology was introduced to provide a topology that allowed more flexibility in layout between channel and gates. Considered the second generation of gate arrays, this new architecture has promoted a substantial advance of the semi-custom design style into the VLSI system integration world, allowing circuits of the order of 1,000,000 gates per chip to be built with a density and flexibility comparable to that achieved in full-custom design. Because of its density and flexibility, the inherent hierarchy of the circuits can be more easily exploited. This is a very important feature, since as a semi-custom environment has a reduced flexibility compared to the full-custom environment, the designer should be able to exploit the flexibility existing at higher levels to improve speed of the design and produce more dense and regular circuits. Because of the possibilities in the physical layout of sea-of-gates, new CAD tools have to be developed to deal with the extra complexity and high level of integration required. For physical design of VLSI chips, and especially for array technology such as sea-of-gates a good placement is critical, since it should be able to guarantee 100% routability or close to it. Sea-of-gates
architecture is flexible in cell positioning, but they do not allow as easy re-positioning of cells in the chip image as other technologies do.

Layout problems such as placements are in general NP-complete[9]. Many heuristics have been proposed to deal with the layout of large circuits, including those based on: analogy with physical laws, analytical techniques, biological phenomena, point-module placement and macrocell placement, constructive and iterative techniques, or structure based approaches with or without slicing[3, 9, 10].

Despite the success of some of these algorithms many of them have problems in achieving good results in the placement of the macrocells in the sea-of-gates array because they ignore important physical parameters in the early stages of the layout. Also, traditional placement systems require a long post-processing time to replace or re-size macrocells after the global placement, and to adjust the routing to achieve an acceptable result. A new approach that is more sensitive to connectivity and geometric constraints, is likely to produce more efficient layouts in a shorter time. There is a clear tendency in recent work to create more complete models, which deal with more parameters simultaneously to improve the layout of chips[6].

A new hierarchical placement methodology is suggested, which takes into account all the necessary geometric parameters, shapes of macrocells, their connectivity and routability within the circuit simultaneously. It has been shown to be able to produce good results in less time, since post-processing for adjustment of the layout can be avoided.

2. Outline of the methodology

This placement method follows recent practice in being performed simultaneously with the global routing[4, 10]. The system uses a hierarchical, constructive force-directed algorithm approach based on an analogy with a new physical model that presents a complexity proportional to \( n^2 \) (n= number of cells to be placed). This more sophisticated physical analogy is based on an electrostatic system and takes into consideration the connectivity, routability and geometric aspects of the macrocells concurrently, the aim being to produce more refined layouts with no need for post-processing. The physical model is explained in the next section.

2.1 Analogy with a physical model

The analogy is between a capacitor of parallel plates, with a dielectric slab between them plates(figure 1a) and the placement of macrocells in slices with different levels of connectivity(figure 1b).

The inclusion of a dielectric slab between the plates of the capacitor, which has an area \( A \) and keeps a distance \( d \) between them, affects the resultant force between the two plates. This resultant is the sum of the force due to free charges(\( F_{\text{free}} \)) on the conducting plates, plus the force(\( F_B \)) due to the induced bound charges on the dielectric surfaces(\( d_B \)). As a result, the resultant force(\( F_r \), figure 1a) is smaller than that of the free charges alone. Taking into account Gauss's law, the resultant force as a function of the parameters above and the dielectric constant \( k \) is given by \( F=F_{\text{free}}/k \).
In our analogy, we define pseudo capacitors as those created when two macrocells face each other within the array during the placement procedure. So, equivalent parameters to those found in a real capacitor as depicted in figure 1 are defined in the following section.

2.1.1 Parameters in the analogy

- The electric free charges on the plates of the capacitor are represented by the common nets (nc) between the new macrocell and the macrocells already placed in the chip.

- The area of the capacitor(A) is here represented by the length of the one of the new macrocell sides facing the neighbouring macrocells which makes up the other plate of the pseudo capacitor (horizontal or vertical direction). So, the area is represented either by the width or by the height of the new macrocell. In each case the other dimension is considered to be a grid unit.

- The distance (d) between the two plates is represented by the average distance between the centres of the new macrocell and its neighbours. This distance is considered as a metric d=|x1-x2|. Neighbouring cells represent macrocells that share common co-ordinates (x- or y- co-ordinates) in the chip.

- The Force: In the analogy to the capacitor with dielectric slab, the force has two components in each direction in the chip (vertical or horizontal).

2.1.2 Forces of attraction

The forces of attraction are used as an analogy for the physical parameters of the behaviour of the macrocells within the chip. They are classified as F_{nc} and F_{b} and are depicted in figure 1.

- F_{nc}: This component represents the ideal attraction force action between a new macrocell (macrocell A) and its neighbours. In this case all common nets
between the new macrocell and the already placed macrocells, represented by macrocell B, keep their y-co-ordinates (horizontal force) or x-co-ordinates (y-direction) within the limit of the new macrocell. This ideal force is then given by \( F_{nc} = nc^2 A/d \).

- \( F_b \). This force represents the influence of those common nets which also connect either the neighbouring or other placed macrocells with the new macrocell, but whose y-co-ordinates, or x-co-ordinates are not within the limits of the new macrocell. This component contributes to the decreasing of the resultant force because of the lower effective connectivity between the common nets.

2.1.3 Connectivity constant

The effective connectivity of the nets in macrocells is measured by a parameter \( \delta_{nc} \), called relative connectivity constant, whose effect is comparable to that of the dielectric constant in a real capacitor. \( \delta_{nc} \) is usually a maximum for nets belonging to the set in \( F_{nc} \) and smaller for those in \( F_b \). Therefore, considering the effect of the pseudo dielectric slab that is here characterised by this new physical parameter \( \delta_{nc} \), the resultant force between the new macrocells and those already placed is given by \( F_r = \delta_{nc} F_{nc} \), resulting in \( F_r = \delta_{nc} A/d \), with \( d \) usually different from \( nc \). This force is slightly different from that in a real capacitor or its capacitance, but the analogy and parameters described lead to an effective placement of macrocells in a sea-of-gates environment.

\( \delta \) represents the influence of the relative connection between cells. This connection depends on the relation between the number of common nets in the new macrocell and those from macrocells already in the circuit. So, each new pseudo capacitor created with the placement of a new macrocell presents a different connectivity constant, which has a major effect on the layout. \( \delta \) is represented by a number, taken from experiments, which depends on the physical relative position of the new macrocells and its neighbouring macrocells, their nets and pin positions (pin-co-ordinates) within the slices. Individually, \( d \) can have 4 different values and interpretation depending on the direction of the force applied on the macrocell and global routing adjustment. The values for \( d \) represent the level of connection between two pins of a net in different macrocells. We define different weight for these levels of connection. The minimum value for \( \delta \) is 0, that represents no connection between the nets from the new macrocell and macrocells from placed slices. The maximum connection happens when a net from a neighbouring macrocells is routed through the new macrocell according to the global routing strategy. This net can be a common net or a crossing net whose co-ordinates are kept within the co-ordinates of the new macrocell. It represents the best procedure for routing and the value for \( \delta \) is 1. However, because it is not always possible have such regularity in the routing, different weights for different global routing adjustment have to be considered. Then, we define two new values that represent two other levels of connection. \( \delta \) equal 0.5 is related to nets that have their pins in the new macrocell and in macrocells in placed slices, but the macrocells in the placed slices are not neighbouring macrocells. The last level is an intermediate level, \( \delta \) is 0.75, which means the pins belong to neighbouring macrocells, but
because the global routing strategy, they cannot be directly routed on the new macrocell.

Figure 2 shows the different values for $\delta$ in both directions of the array (vertical and horizontal).

![Diagram showing connectivity constant $\delta$ in the horizontal and vertical directions](image)

2.1.4 Objective function and internal energy

Another important parameter in our methodology is the objective function. A cost function or objective function consists of a method of measuring the performance of the placement[13]. Most of them are based on the sum of the total wire length[14], but other objective functions can also be applied such as cell density[15], channel density[16], area utilisation[17], with varied interpretations and equations. Penalties such as overlap, feed through, chip area, and so on, can also be considered. These strategies are related to one other in such a way that in general, the main objective of the placement, minimum wire length and chip area can be achieved. The attraction force represents our objective function. It takes into account the electrical connectivity among the macrocells, dimensions (size and shapes) and routability of the new feasible macrocell and simultaneous area optimisation. The resultant force is the sum of two perpendicular components, $F_x$ and $F_y$ respectively as depicted in figure 3. The force is locally maximised by choosing a macrocell that optimises all geometric and topological parameters for the available space chosen in the grid. Although this may lead to a local increase in some forces, the resultant for each macrocell in the circuit tends to minimum. On the other hand, as the energy changes with $lnx$, where $x$ also represents the medium distance for the nets between two macrocells, there is a close dependency between energy and net length and vice-versa. So, as we can see, the system tends to minimise the net lengths in the circuit and the internal energy of the chip, as desired in a good layout.

3. Overview of the system

A system called SISTEMA was developed in order to implement our methodology. The software is written in PASCAL VAX-VMS. SISTEMA supports:
- Circuit Netlist Decoder. This module transforms the input circuit file in ASCII structurally described, converting all circuit specification, represented by macrocells from the main library or from the user libraries, into special files which will be used for the creation of the layout database. The input file specification is based on a HDL hardware description language description which is compatible with that one from Plessey (CCL)[8]. The compiler also:
  - checks the availability of the libraries used in the circuit description;
  - checks availability of macrocells on the libraries;
  - checks that the number of net calls is correct;
  - checks the interconnection pattern for connectivity;
  - produces the path identifications of the hierarchy of the circuit.

- Libraries. The libraries can be divided into two different classes, System library and user library. As our system has been used in two different environments, Ocean and Plessey, a set of different libraries has been used for each of the environments. The libraries are defined as:
  - System library. The system library comprises primitive macrocells characteristics from Ocean[2] or Plessey system[8].
  - User library. The user libraries keep special macrocells (multipliers, address, ALUs, etc.) implemented for the user. These macrocells are available for any further project implemented by the user.

- Data-structure. SISTEMA uses a data-structure based on Corner-Stitching[18] methodology for rectangular blocks. This method improves the performance of the algorithm since it promotes a fast search for macrocells in the chip, an easy deletion and addition of new macrocells.

- System user interface. SISTEMA provides a very simple interface with the user that enable the layout phases to be easily manipulated by a multi-menu display. The designer can interact with the system and perform functions such as:
  - to check macrocells characteristics;
  - to produce the placement and global routing of part of the circuit or whole circuit automatically;
  - to change template size (width and height) in order to optimise the floor-planning at some stages during the layout.

- Layout tools manager. This module manages the placer and the router.

4. Placement of the macrocells

The placement of macrocells is performed hierarchically in different levels. In each level the macrocells are fitted into vertical slices whose structure belongs to the class constructed by successive augmentation.

The placement technique can be better explained by reference to the algorithm below:
Let us consider, initially, a set of possible neighbouring macrocells from the places slices $M_{ng} = \{ m_1, m_2, m_3 \ldots m_k \}$, a set of unplaced macrocells $U = \{ u_1, u_2, u_3 \ldots u_n \}$ and a set of suitable spaces at some time during the placement $S' = \{ s_1, s_2, s_3 \ldots s_k \}$.

(Algorithm to calculate the best macrocell to be placed into a new slice which already contain macrocells, as a function of the best objective function value)

begin
  {initial conditions}
  a = 1; \{ first element of U - set of unplaced macrocells \}
  c = 1; \{ first element of S' - set of available free spaces\}
  \{calculus of the best objective function\}
  objective_function = 0;
  \{ initial value for objective function\}
  while(a ≤ n) do ( a = 1, \ldots n)
  begin
    while(c ≤ k) do ( c = 1, 2, \ldots k)
    begin
      if(s_c ≥ u_a) then
        \{ u_a satisfies the geometric constrains\}
        begin
          \{ u_a ∈ U, s_c ∈ S' \}
          $M_{ng}' = \text{find_neighbouringMacrocells}(u_a, M_{ng}(s_c))$;
          \{ neighbouring macrocells for u_a in that position; M_{ng}' ⊆ M_{ng} \}
          new_objective_function(u_a, M_{ng}');
        \{new objective function\}
        if(new_objective_function > objective_function) then
          objective_function = new_objective_function;
        end; \{if\}
        c = c+1;
      \{ try another empty available space\}
      c = c+1;
    \{ get next unplaced macrocell \}
  end; \{while\}
end; \{while\}

The procedure stops when all possible macrocells were tested for all free space in the slice. The macrocell that presents the best objective function as a function of the force attraction approach is then placed in the location found.

The minimum connection length as a criterion for selection of a candidate set can be approximated by maximisation of connectivity between preceding and succeeding slices[11]. The area is also minimised dynamically because of the simultaneous process of compaction during the placement.

4.1 Macrocells

Unlike standard cells, macrocells can present different aspect ratios. These macrocells do not overlap at any time during the layout of the chip and so they require some geometrical analysis at the time a new macrocell is to be placed. They can present pins inside or around their border and as sea-of-gates macrocells, they also, in general, present a certain number of vertical
and horizontal feed-through which is used to improve the placement and so the density of the design.

Each macrocell specification in the libraries comprises the following series of parameters:

- **cell name.** Each cell has a unique cell identification in the library;
- **function.** Identifies the function of the cell, such as mux, ands and so on;
- **height.** Height of the cell;
- **width.** Width of the cell;
- **hor-ft.** Number of horizontal tracks available for routing;
- **vert-ft.** Number of vertical tracks available for routing;
- **cell-pin_file.** This parameter keeps all pin specifications of the cell.

### 4.2 Slices

The slices do not necessarily have a regular shape and are created and placed from left to right until all cells are arranged in a grid, as shown in figure 3. The layout is then produced constructively, from left to right, one slice at a time, satisfying the constraints of geometric fit, connectivity and routability. The slices grow vertically taking into account the geometric limits of the chip. The placement of the cells starts from a seed that is first placed as a function of the attraction force with the slices already placed. The resultant force in this case has only a horizontal component ($F_x$) since there are no other macrocells in the slice ($C_1$, figure 3). The other macrocells are then placed in the new slice as a function of the macrocells already placed in previous slices and the macrocells in the new slice ($C_2$, figure 3b). Now, $C_2$ presents two components $F_x$ and $F_y$. The vertical component only exists when there is more than one macrocell in the same slice ($F_y$-figure 3b).

![Figure 3: Inclusion of new macrocells in a new slice](image)

Although the area and distance depend only on the neighbouring macrocells, the connectivity constant depends on the total connectivity of the macrocell with the whole cells on the previous slices (horizontal direction-$d_x$) and the new slice (vertical direction-$d_y$). After each slice has been implemented, a new space is allocated for a new slice and so on.

The first slice receives a special treatment. Its macrocells have only a horizontal component and the force are calculated considering pseudo
macrocells which have the same dimension of the new macrocells (figure 3a). In this case the connectivity constant is equal to the number of common nets between the new macrocell and the external connections. Their vertical components work as described previously. The macrocells in the first slice can also float vertically in order to adjust the macrocells in the slice until its limit is reached. Auxiliary slices are also used to manage the free space available to place new macrocells in new slices. These slices, up-slice and down slices, also reduce the number of tiles to the represented in the datastructure.

4.3 Compaction of the slices

Usually compaction is performed after the relative placement of the macrocells, requiring post-processing to optimise space without overlapping[12]. In contrast, this methodology performs compaction and global routing during the placement. So, each new macrocell is shifted left as far as is possible toward its neighbouring macrocells, and upward or downward as is appropriate to its relative location within the new slice as depicted in figure 4a. This approach reduces area and produces more regular slices.

5. Global routing

The global routing problem, sometimes called loose routing, has as its goal the creation of a routing strategy in which each connection between pins of a net in the circuit is assigned to a routing region with enough feed-through aiming at a minimisation of the total wire length. SISTEMA treats this problem simultaneously with the placement of macrocells. The adjustment of feed-through for routing in regions of congestion is performed in two distinct sub-classes, which take place in different phases of the layout. In congestion areas a free space can be incorporated to the macrocells in order to allocated enough space for routing (figure 4). This space allocation is done in the two orthogonal directions during the placement of the macrocells as follows:
- Horizontal global routing. This routing adjustment is performed in the x-direction and each time a new cell is to be placed, considering aspects such as number of free horizontal tracks, routability and geometric constrains of the macrocells (macrocell C2, figure 4b).
- Vertical global routing. In the y-direction, this adjustment is carried out after the completion of each slice in the chip, providing enough vertical feed-through in each slice. It is also performed on previous slices, when
after the compaction process, the macrocell is absorbed by the previous slice. This is necessary to preserve the routability of the slice (macrocell C₂, figure 4c).

6. Experimental results

SISTEMA was implemented in Pascal/VMS on a DEC-VAX system. Its results were compared with those produced by Plessey system using the family CLA60000[PDS90] for sea-of-gates and Ocean[Gro93] using different basic cell images with different grid dimensions. Some experimental circuits were created and its layout generated automatically for the three systems as depicted in table 1.

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<th>No. Nets</th>
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Table 1: Results of the automatic placement in the three systems

The result shown above indicates that this methodology is able to produce layout as good as or better than other systems for sea-of-gates.

The smaller area achieved by SISTEMA is a function of the simultaneous process of compaction which tries to reduce wasted space, and the global routing strategy which is able to preserve a good routability.

7. Conclusion

A new method for physical interpretation of the problem of macrocell placement in sea-of-gates has been discussed.

The model has been implemented as an automatic layout tool and demonstrated in comparison with tools using more conventional underlying models.

The model proposal has been shown to be able to produce better results because of its ability to explore parameters not conventionally used in the same environment.

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8. Acknowledgements

This project was supported in part by Federal Agency for Post-Graduate Education, CAPES in Brazil and by the Computing Centre at Federal University of Pernambuco (NP/DUFPE-Brazil). The authors also would like to thank Paul Stravers and Patrick Groenveld at Delft University for their support on Ocean System.

9. References